Dynamic Reconfigurable TCAM with Low Power Consumption

Final Project Report

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I. Introduction

As a router and a switch are advanced, it has started to support Software Defined Network (SDN) technique which enables dynamic, programmable, and efficient network configurations. Since proposed in 2009, it has become the most promising architecture for large-scale networks. SDN protocols (e.g., OpenFlow [1] from Google) in a router or a switch require rule tables to classify packets floating around the networks. It basically checks a specific field in the packet and compares with rules on the table. For the comparison, most of architecture uses Ternary Content Addressable Memory (TCAM) [2].

Problem Statements and Motivation

However, using TCAMs on SDN protocols has two main limitations:

(1) Different length of rules in the protocols - Because of the length difference of the rules, many architectures reserve long memory address spaces which should be at least same length as the longest rule. However, if the long rules are not many in the rule table, we waste all the empty remaining memory spaces in short rule address spaces.

(2) High power consumption due to the use of TCAM - General TCAM design consumes high power consumption, and the details about this limitation will be covered in the following section II.

Goal

To solve the aforementioned limitations, our group proposes a new TCAM circuit design. A core idea of our implementation is from previous paper [3]. Due to the limited padframe space, we scaled down to less number of bits and rows on our design.

Here are contributions (impacts) of our design:

- Enabling dynamic reconfiguration for number of bits to search by implementing mode scheme
- Combination of NAND TCAM and NOR TCAM lowering power consumption and still giving good filtering performance
- Improve throughput using a pipeline between NAND gates and NOR gates

On this report, we demonstrate how feasible and practical to use our design by explaining from high level to all the way down to low level (e.g., Pins used) and by showing simulation results and performance.

II. Background on TCAM

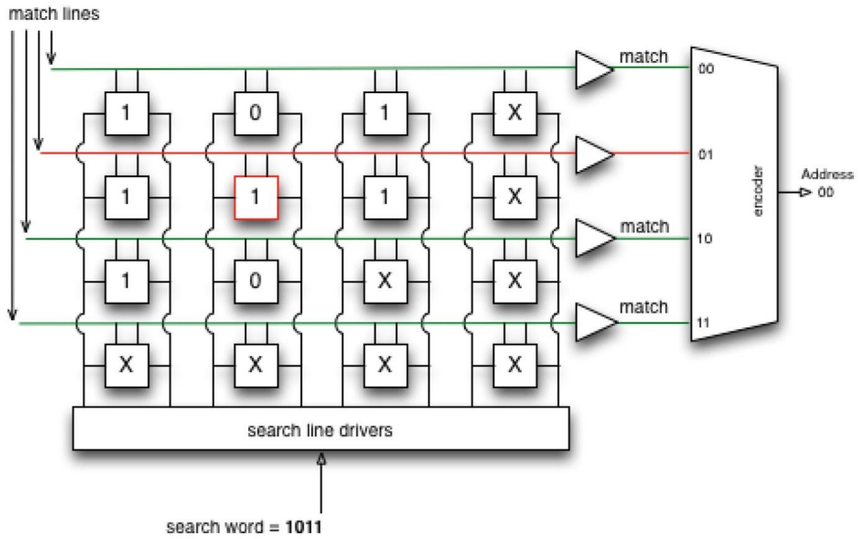


Fig. Example 4-Bit Search Operation using TCAM

Ternary Content Addressable Memory (TCAM) is a more flexible type of CAM and allows masking bit. For the masking, TCAM has extra third type bit which is “don’t care”. It is famous and widely used for fast searching operation (e.g., IP matching) because it can be done in single clock cycle. However, it is also known for expensive (in space size) and highly power consuming design. Because of parallel usage, it consumes power even when it’s not matched. In the above figure, let’s say there are 4 bits to check, and the given input is 1011. On second row, second bit is not matched, and there is no point to check the rest bits, but current TCAM designs still consider the rest bits and consumes unnecessary power there.

III. Circuit Design

In this section, we talk about overall design and details of each component including screenshots.

Overview of Our Design

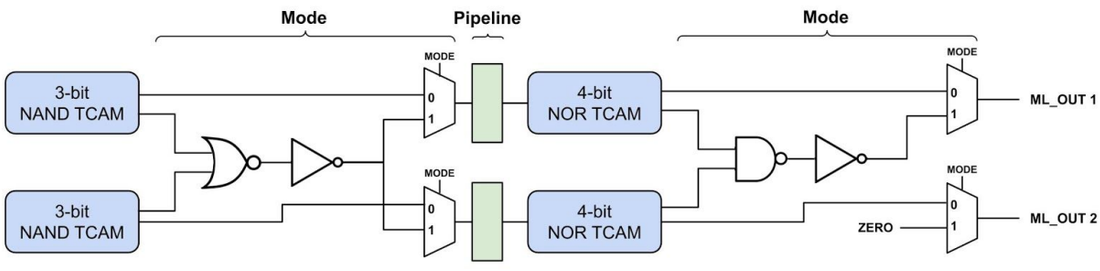


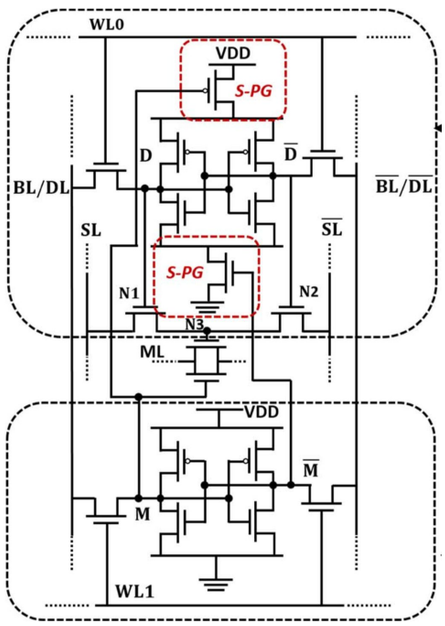
Fig. Overview of Design

The figure shows an overview of our circuit design. As mentioned in introduction, we scaled down to less number of bits, 3-bit NAND TCAMs and 4-bit NOR TCAMs. Also, we implemented two rows (7bits in single row) in the design. However, scaling up from our design will not take much time, and it is just engineering work.

Between NAND TCAMs and NOR TCAMs, we inserted mode multiplexer and pipeline. Pipeline divides search operation into 2 stages, separate NAND TCAM search and NOR TCAM search, and this almost doubles overall throughput. Mode multiplexer enables dynamic reconfiguration of number of bits by joining two rows. In mode 0, two rows operate individually, and those join together when the mode is 1. In rest of this section, we talk about further details about each component.

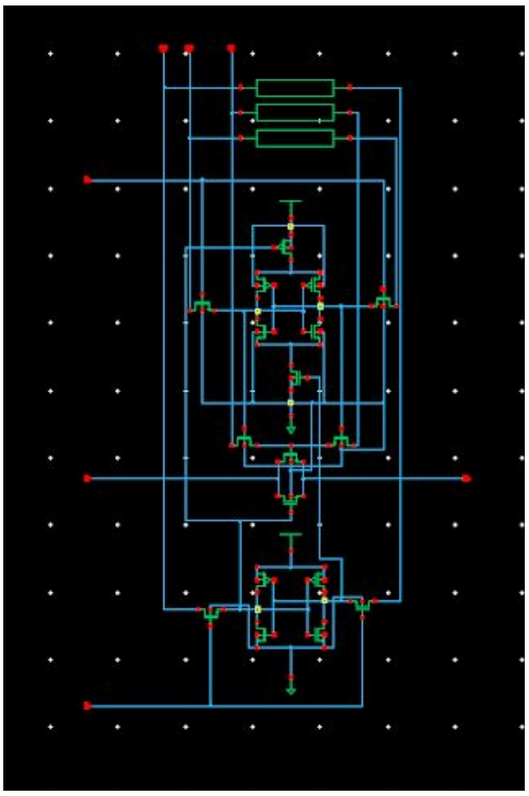
a. NAND based TCAM

NAND based TCAM consists of two SRAM. One SRAM is used to store the data bit. The other SRAM is used to store the mask bit. BL is used as a data input bit and mask bit depends on the WL0 and WL1 write lines. WL0 and WL1 are inverted with each other when one is turned on others are turned off. When WL1 is high the BL acts as mask bit and WL0 is high the same BL is acting as a data bit. BL and DL are feed to the NMOS transistor as shown in the figure. The SRAM which we used in the circuit is 6T SRAM. The inverted input of BL and DL are feed to the other side of the circuit.SL line is used to feed the search bit to the circuit. ML is used to give the output low or high depending on the match or mismatch case. The Transistors in the red box are used as a self-power generating transistor which controls the power consumption of the circuit.

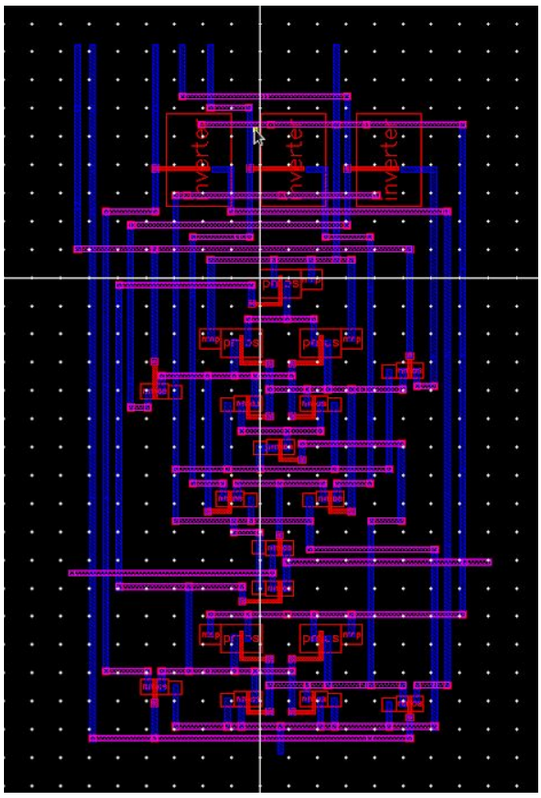


Flow: The circuit is precharged before proceeding with the evaluation part. First, the WL0 is high and WL1 is in low and BL acts as data input bit. Once data is fed in the top SRAM circuit, when WL0 is low the data fed is rotated in the top latch the BL will act as mask bit with WL1 turned on. During the evaluation phase, the SL is fed as shown in the figure. One of the N1 or N2 will be turned on depends on the data bit 0 or 1. When the data bit 0 N2 is turned on and when the data bit is 1 N1 is turned on passing SL or SLB to the transmission gate present in between the two blocks. When the Mask bit is turned off and the data bit and search bit matched then the transmission gate is turned on and the precharged voltage is discharged, if it is mismatched that transmission gate is turned off and output stays high. So in NAND TCAM output low represents match case. When a mask bit is enabled independent of data bit and search bit the transmission gate is turned on and output is low . so it always is in the match case. When a mask bit has enabled the transistors in the red box turned on and turn off the top circuit. Since at that time output is independent of the data bit. the power consumed by top circuit is Wasted so this can be reduced for low power consumption. This circuit is implemented in schematic view and output is verified and the same circuit is implemented in layout. After verifying DRC the circuit is extracted and output is verified and did the LVS match to make sure it is matched with schematic.

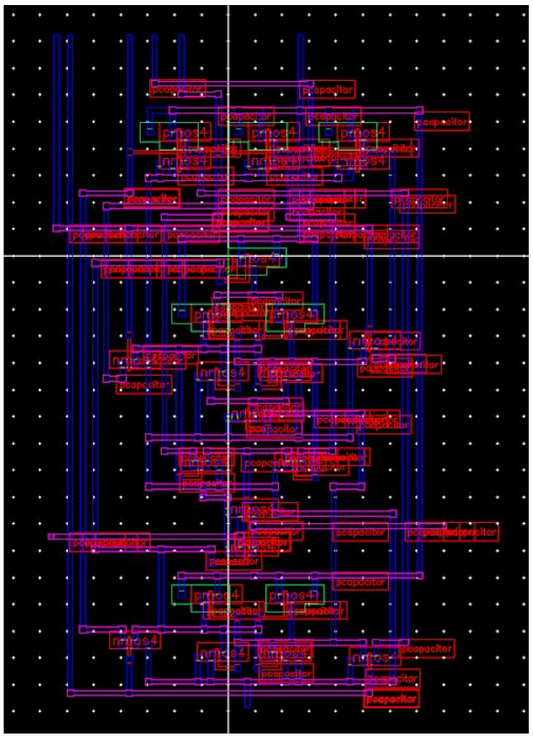
Schematic View



Layout View



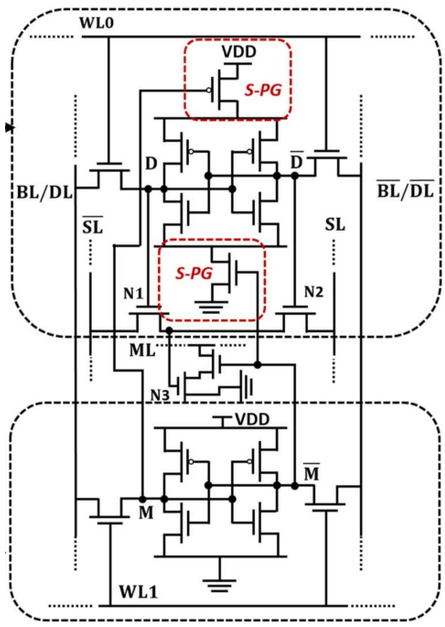
Extracted View



b. NOR based TCAM

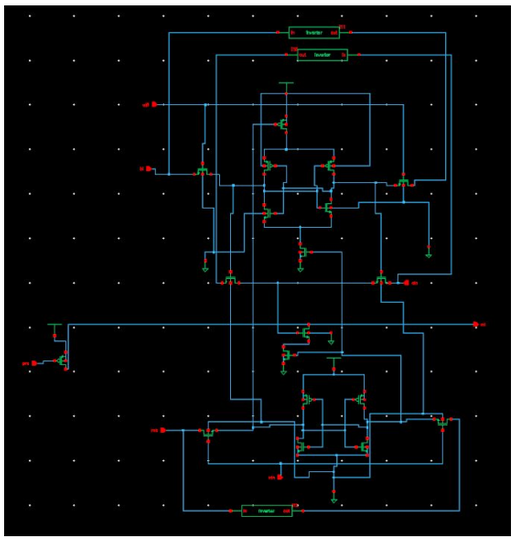
NOR based TCAM consists of two SRAM. One SRAM is used to store the data bit. The other SRAM is used to store the mask bit. BL is used as a data input bit and mask bit depends on the WL0 and WL1 write lines. WL0 and WL1 are inverted with each other when one is turned on others are turned off. When WL1 is high the BL acts as mask bit and WL0 is high the same BL is acting as a data bit. BL and DL are feed to the NMOS transistor as shown in the figure. The SRAM which we used in the circuit is 6T SRAM. The inverted input of BL and DL are feed

to the other side of the circuit.SL line is used to feed the search bit to the circuit. ML is used to give the output low or high depending on the match or mismatch case. The Transistors in the red box are used as a self-power generating transistor which controls the power consumption of the circuit.

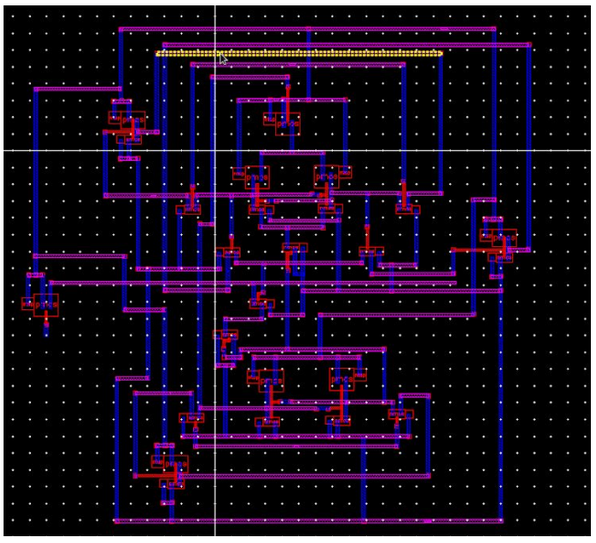


Flow: The circuit is precharged before proceeding with the evaluation part. First, the WL0 is high and WL1 is in low and BL acts as data input bit. Once data is fed in the top SRAM circuit, when WL0 is low the data fed is rotated in the top latch the BL will act as mask bit with WL1 turned on. During the evaluation phase, the SL is fed as shown in the figure. One of the N1 or N2 will be turned on depends on the data bit 0 or 1. When the data bit 0 N2 is turned on and when the data bit is 1 N1 is turned on passing SL or SLB to the transmission gate present in between the two blocks. When Mask bit is turned off and data bit and search bit matched then the top transistor is turned off and the bottom transistor is turned off and the precharged value stays high if it's mismatched then both the transistors turned on and output stays low. So in NOR, TCAM output high represents match case. When a mask bit is enabled independent of data bit and search bit the bottom transistor is turned off and output is high. so it always is in the match case. When a mask bit has enabled the transistors in the red box turned on and turn off the top circuit. Since at that time output is independent of the data bit. the power consumed by top circuit is Wasted so this can be reduced for low power consumption. This circuit is implemented in schematic view and output is verified and the same circuit is implemented in layout. After verifying DRC the circuit is extracted and output is verified and did the LVS match to make sure it is matched with schematic.

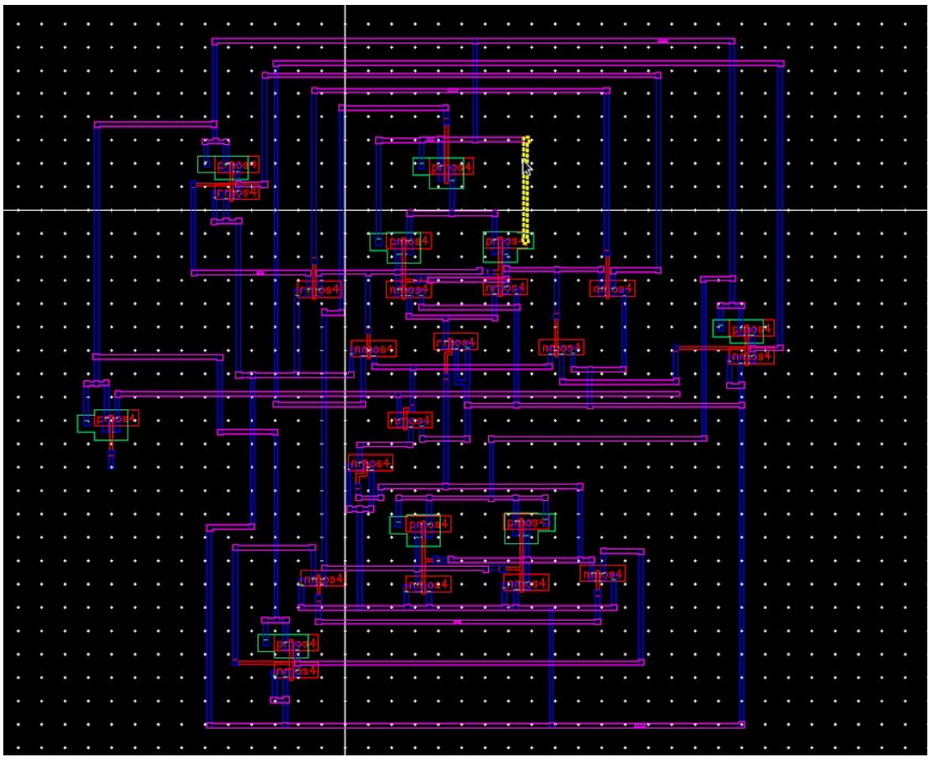
Schematic View



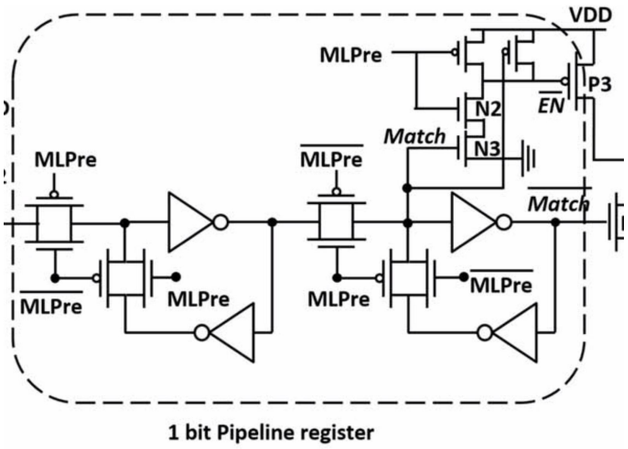
Layout View



Extracted View



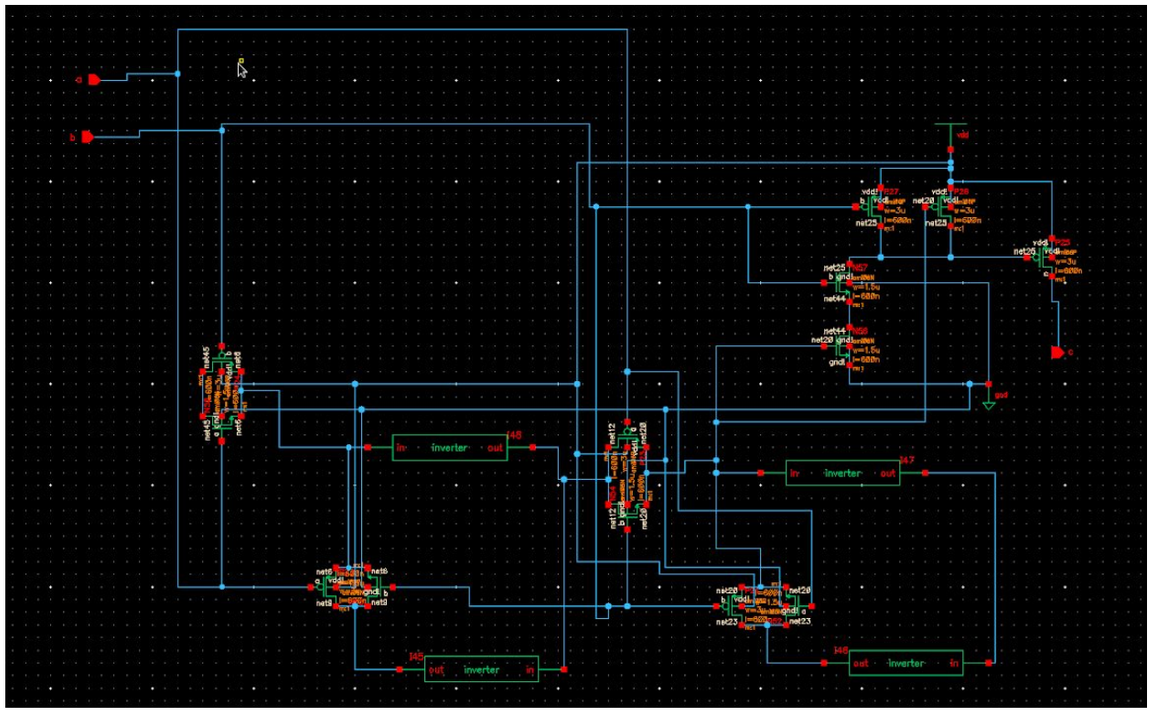
c. Pipeline Register



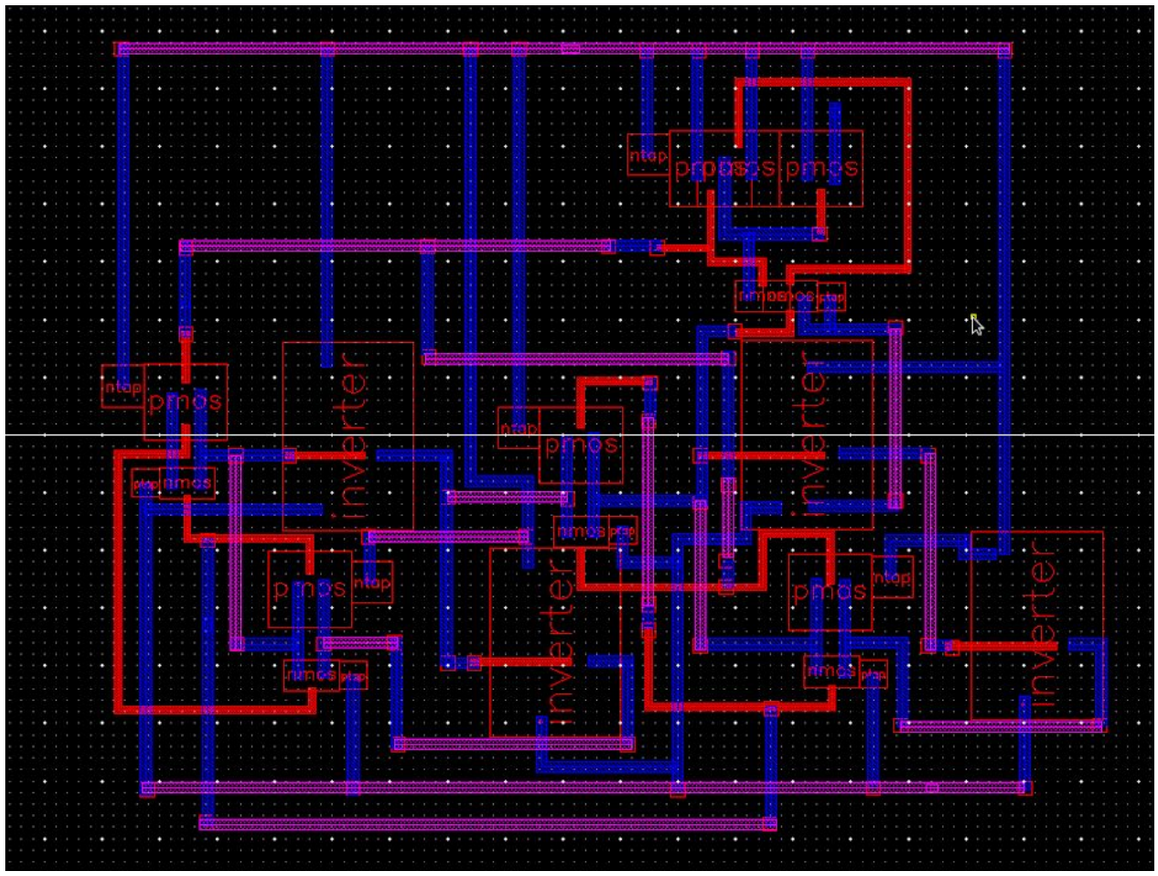
1 bit Pipeline register

The pipeline circuit is used to double the throughput and makes the circuit to work faster. The pipeline register we used in our circuit is a 1-bit pipeline circuit. Which consists of two D flipflops which are of transmission gates. This transmission gate is controlled by the precharge value. It acts as a bridge between the NAND and NOR tcam circuits. This just passes the value of the nand output to the nor tcam. This pipeline register divides into two stages, it's like two d flipflops connected in series. During the evaluation phase the Nand tcam produces the output depends on whether it's matched or not, the first flip flop turned on and data is stored in first flip flop at this time the second flip flop is turned off. During the precharge phase the second flipflop turned on and the data from first flip flop passed to the second flipflop and first flip flop turned off. N3 transistor in the circuit is controlled by match and N2 transistor is controlled by the precharge bit and P3 is controlled is depends on its match or not. When its en is 1 p3 turned on and passes the vdd to nor tcam for further evaluation. During the next evaluation phase, the first set of data is being searched in nor tcam parallelly second of data start searching in nand tcam and output data is stored in the first flip flop. There will be no interference between the outputs of the first set of data and the second set of data. This can be maintained by precharge bit, by turning one flipflop turn on at one time. Like when one flip flop is turned on another flip flop is turned off. Thus the process becomes faster so the throughput is doubled. This circuit is implemented in schematic view and output is verified and the same circuit is implemented in layout. After verifying DRC, the circuit is extracted and output is verified and did the LVS match to make sure it is matched with schematic.

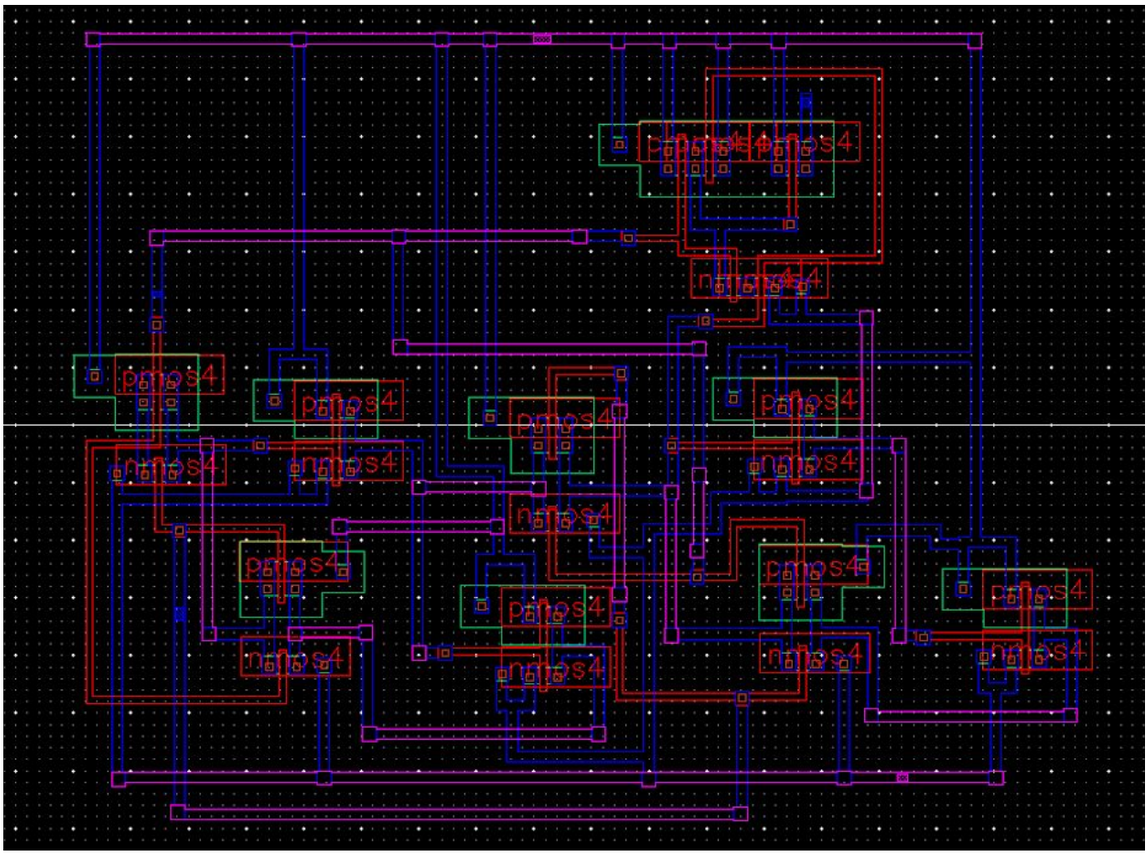
Schematic View



Layout View



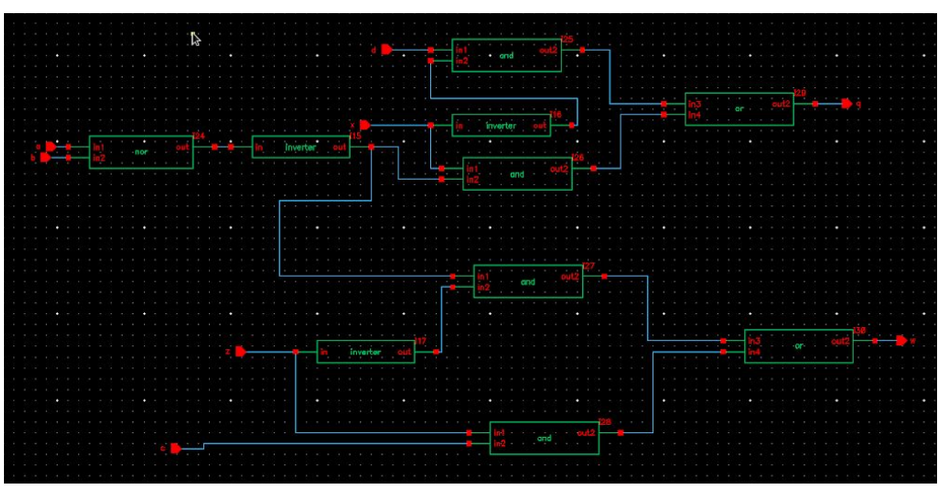
Extracted View



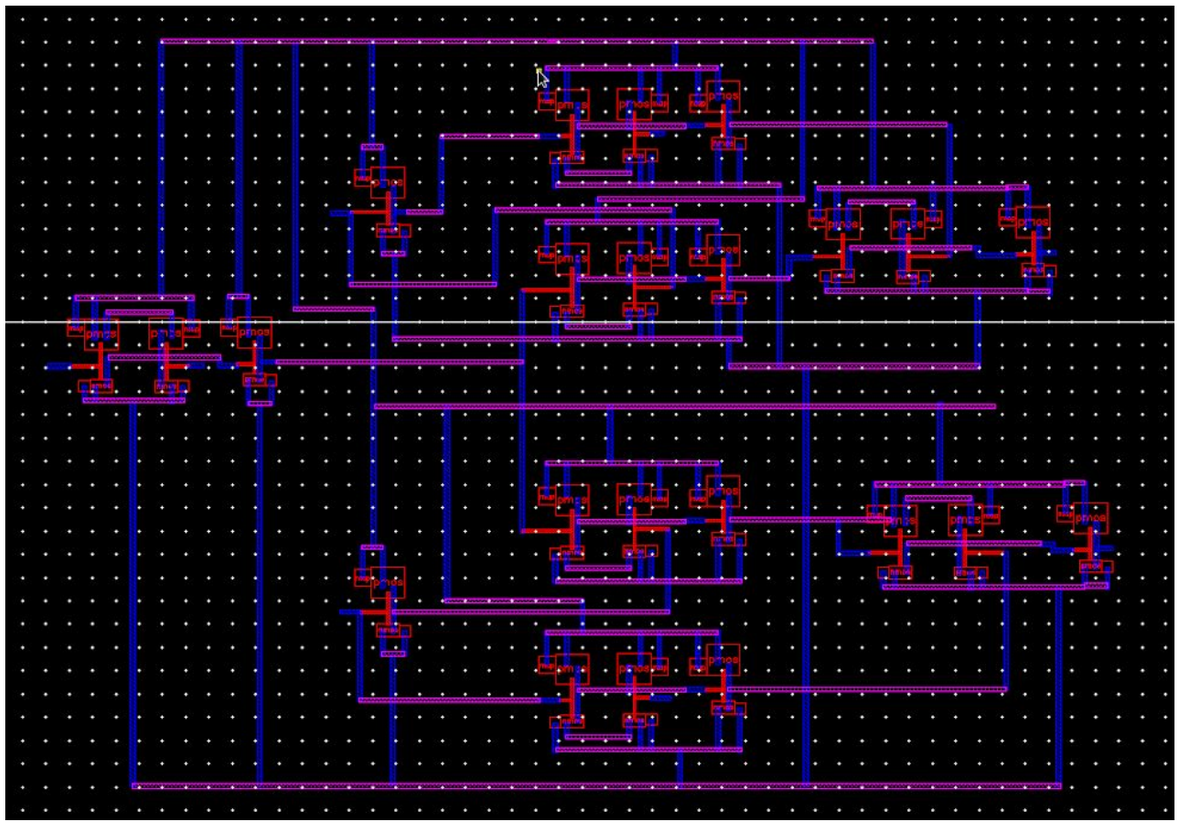
d. Mode Operation

Dynamic reconfigurability which provides a lot of flexibility to the circuit is achieved using this mode operation. The major part of this mode circuit contains multiplexers. A 2 to 1 mux is used to choose different modes. the inputs to the mux are given by connecting circuits whose inputs are from outputs of nand based tcam. When its in mode 0 operation. Each array of tcams acts independently and searches independently. If one of the arrays is mismatched it does not affect all arrays its output alone is changed. When it is in mode 1 operation the two arrays are dependent on each other so if one of the arrays is mismatched the whole circuit is mismatched. For example, if each array seven bits in mode 0 the first 7 bits output is independent of the second array 7 bits. But in mode 1 only when 7+7 = 14 bits are matched the output is matched. This mode circuit used two times in the circuit. one at the end of the nand tcam and another one at the end of the nor tcam. This circuit is implemented in schematic view and output is verified and the same circuit is implemented in layout. After verifying DRC the circuit is extracted and output is verified and did the LVS match to make sure it is matched with schematic.

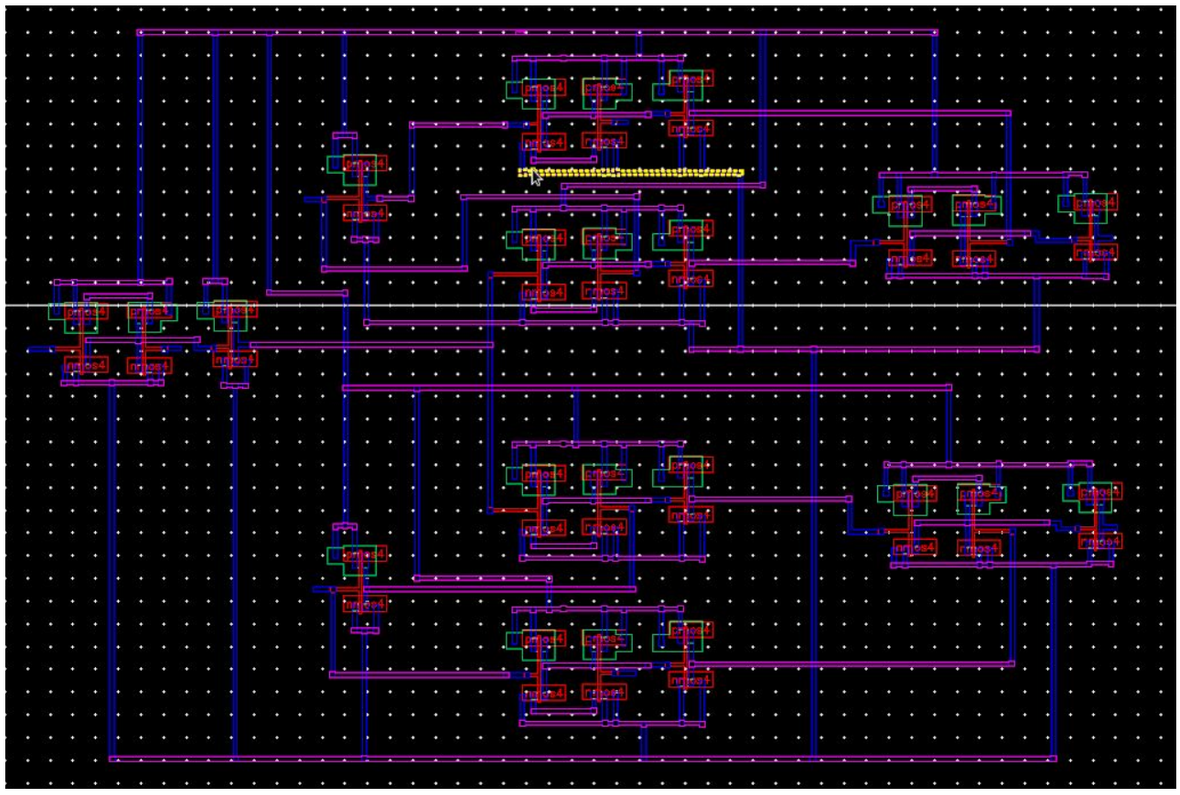
Schematic View



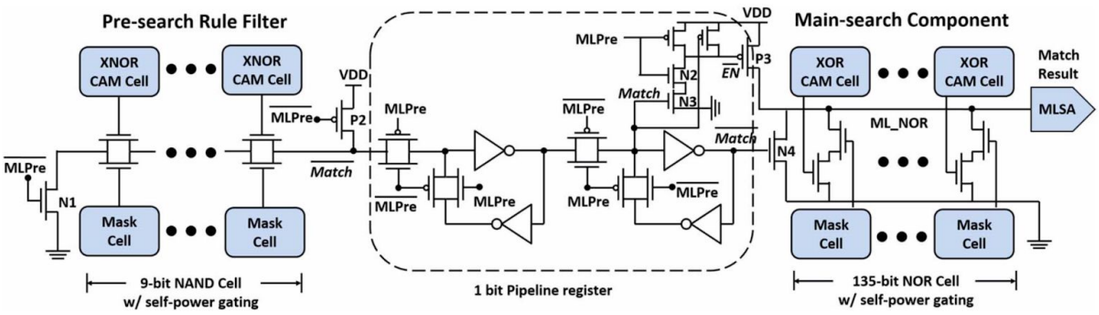
Layout View



Extracted View



e. Full Circuit



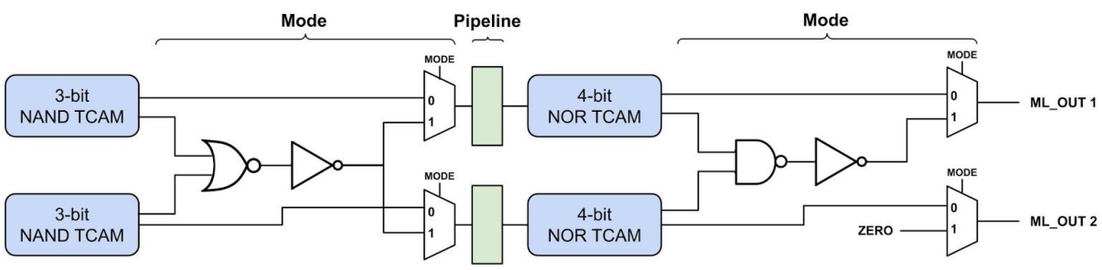
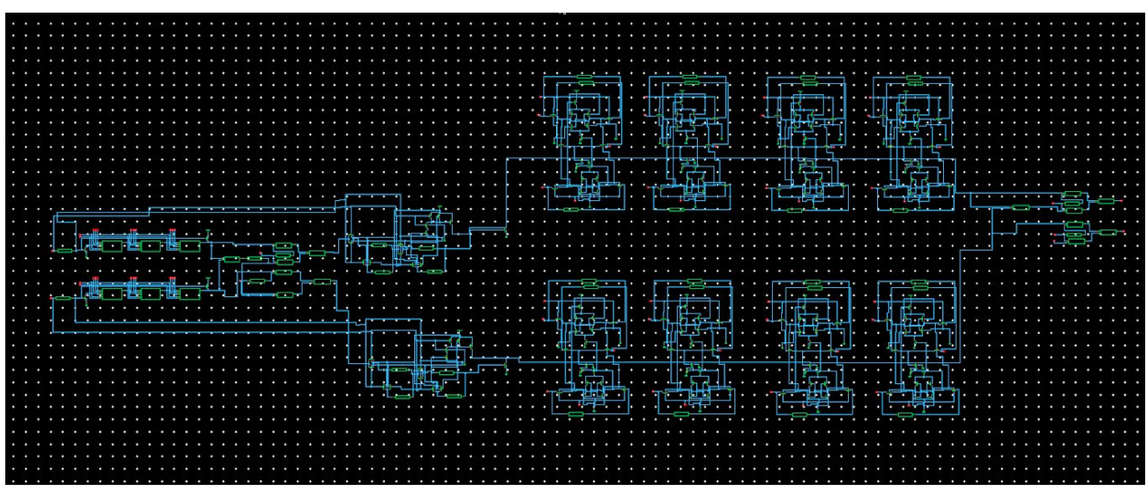


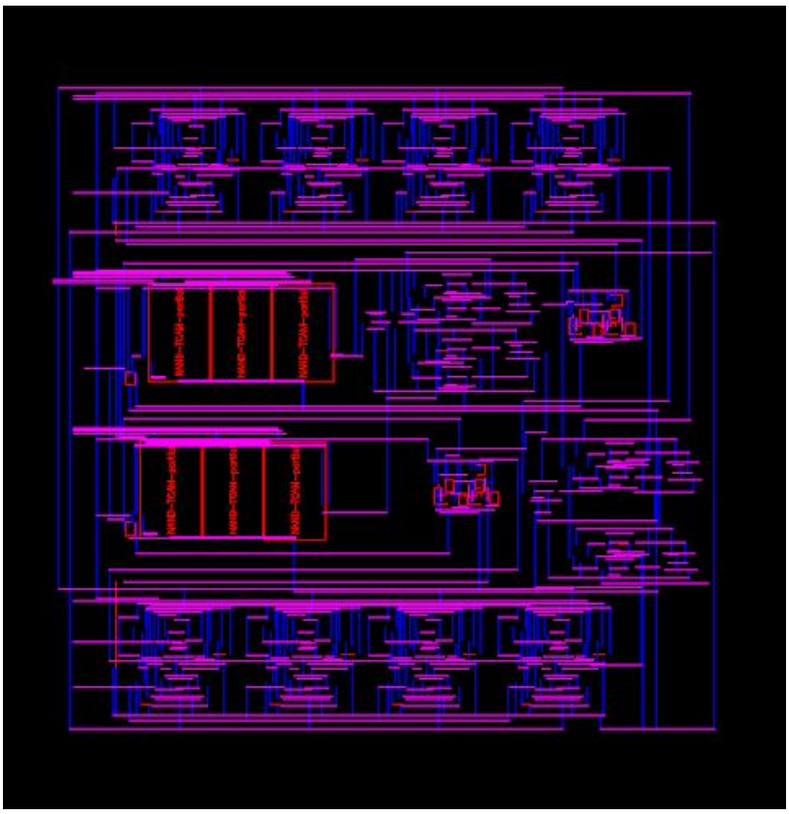
Fig. Overview of Design

The four individual components mentioned above are joined to form the whole circuit so the first the nand tcam does the search operation then the output of two arrays fed into the multiplexer and then the depending on the mode selected the independent outputs or combined output from are fed into the pipeline circuit.Then depending on the match or mismatch case the output of a pipeline is determined and feed to the nor based tcam. Again the outputs of the nor tcams fed to the multiplexer and depending on the mode selected the combined output or individual outputs can be obtained. The full circuit is implemented in schematic view and output is verified and the same circuit is implemented in layout. After verifying DRC the circuit is extracted and output is verified and did the LVS match to make sure it is matched with schematic.

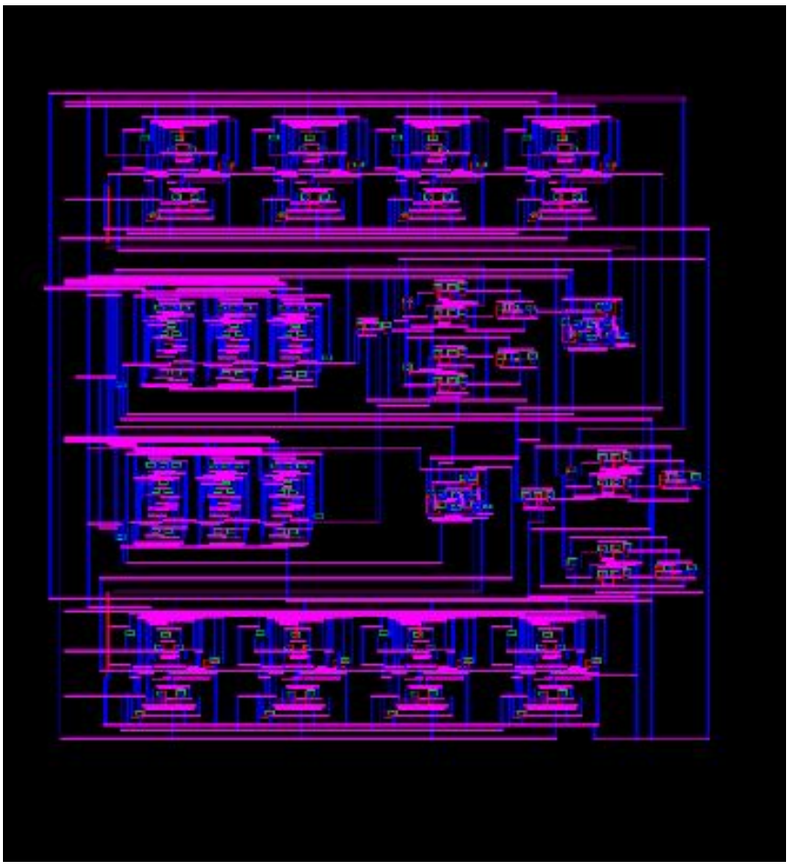
Schematic View



Layout View



Extracted View



f. Padframe

The full circuit is implemented in schematic view and output is verified and the same circuit is implemented in layout. After verifying DRC the circuit is extracted and output is verified and did the LVS match to make sure it is matched with the schematic. Then this circuit is placed in the pad frame after doing necessary adjustments to make it fit in the pad frame. Then it is extracted and output is verified for the last time.

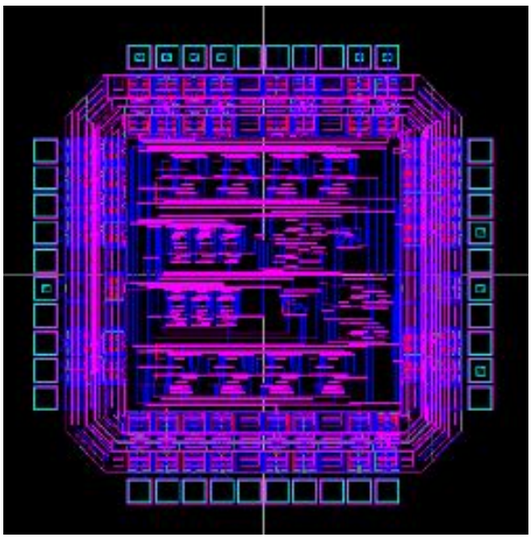
Pins used:

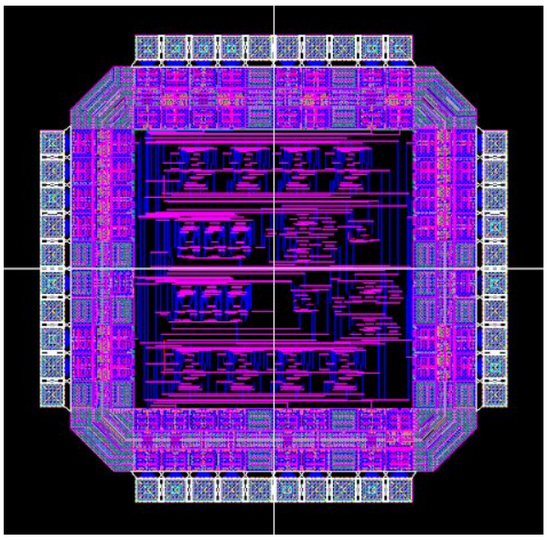
16 Input - 1 WL, 1 ML_IN, 4 SL, 4BL, 4ML, 1 mode, and zero

2 Input/Output - gnd, vdd

2 Output - ML_OUT1, ML_OUT2

Layout View **Extracted View**

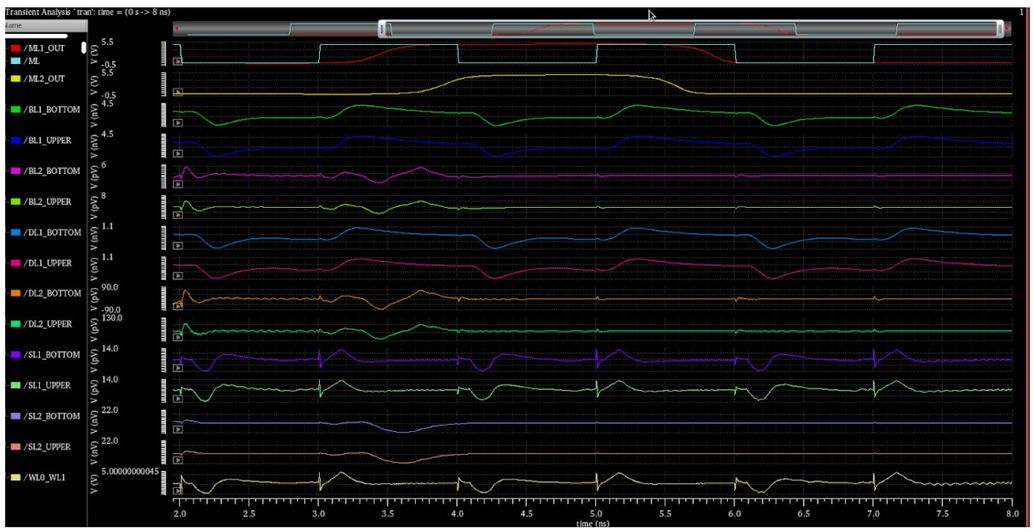




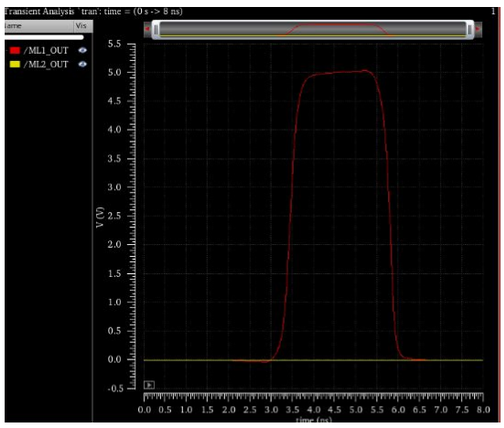
IV. Simulation and Evaluation

This circuit is tested for the various inputs and various mode operations to make sure the circuit is working accurately.some of the resulted are displayed below. To make the graph more clear in most of the circuits we are only just displaying output lines. These simulation results are simulated with the pad frame.

Simulation 1. MODE 0 - Both Match (mask: disabled)



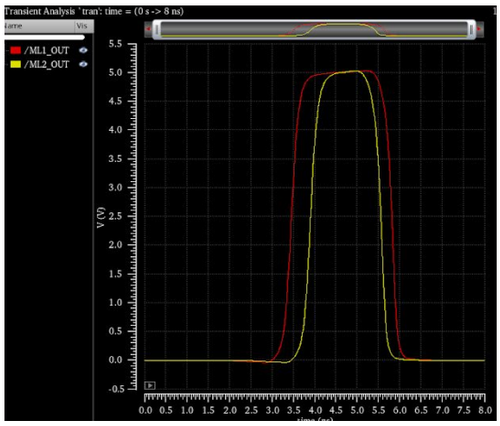
In this test case, we fed the input data and search data for both the array as the same and matched. we disabled the mask bit. we selected mode 0 in this case so the outputs are independent of each other . so we can see two output lines raised high during the evaluation phase.



Simulation 2. MODE 0 - One Mismatch

(mask: disabled)

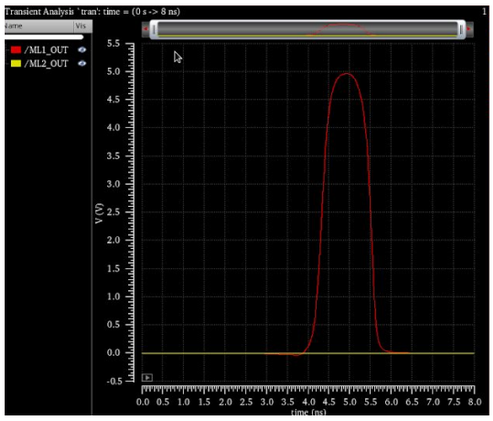
In this test case (figure on left), we fed the input data and search data for one array as same and matched but for another array we mismatched. we disabled the mask bit. we selected mode 0 in this case so the outputs are independent of each other . so we can see first output lines raised high during the evaluation phase but second is in low which means mismatch.



Simulation 3. MODE 0 - Mismatch

(mask: enabled)

In this test case, we fed the input data and search data for both the array as different and mismatched. we enabled the mask bit. we selected the mode 0 in this case so the outputs are independent of each other . so we can see two output lines raised high during the evaluation phase.



Simulation 4. MODE 1 - Mismatch

(mask: enabled)

In this test case, we fed the input data and search data for both the array as different and mismatched. we enabled the mask bit. we selected mode 1 in this case so the outputs are independent of each other . so we can see the combined output line raised high during the evaluation phase.

Power consumption: The power consumed by the general TCAM is in order of 456E-6 but the power consumed by the S-PG tcam is around 926E-9.

V. Flow Chart and Work Distribution

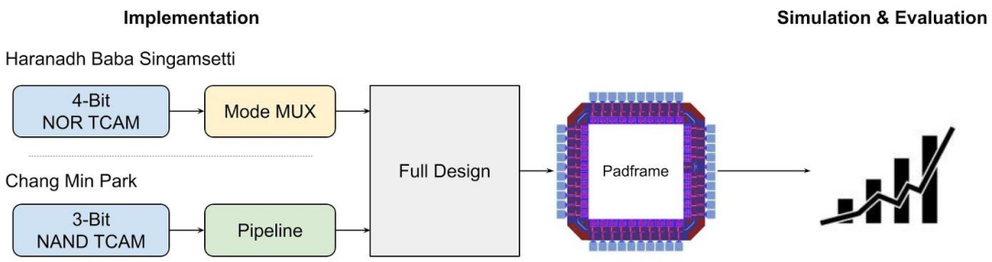


Fig. Project Flow Chart

As shown on above figure, we started with component designs. Baba implemented 4-bit NOR TCAM and mode multiplexer (both schematic and layout), and Chang Min implemented 3-bit NAND TCAM and pipeline (both schematic and layout). From designing full circuit combining those components, we worked together.

VI. Conclusion

To sum up, for our project, we investigated how to design a TCAM circuit providing a lower power consumption and also dynamic reconfiguration. There were two main limitations of current TCAM table design. We designed mode scheme to support dynamic reconfiguration for number of searching bits and also designed pipeline to lower power consumption and to increase throughput. From simulation and power consumption evaluation, we successfully show correctness and effectiveness of our design. Lastly, from this project, we have learned whole process of designing a system on chip from transistor level to actual padframe layout, and also we could implement circuit components (e.g., Transmission gate based D flip-flop), that we learned in lecture, on real system.

VII. References

[1] OpenFlow https://www.segment-routing.net/images/hoelzle-tue-openflow.pdf

[2] TCAM https://en.wikipedia.org/wiki/TCAM

[3] Ting-Sheng Chen et al., “Dynamic Reconfigurable Ternary Content Addressable Memory for OpenFlow-Compliant Low-Power Packet Processing”, IEEE Transactions on Circuits and Systems, 2016